UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/710,272 | 06/30/2004 | Bruce Bennett Doris | FIS920030389US1 | 4271 |

48144 7590 12/14/2009

MCGINN INTELLECTUAL PROPERTY LAW GROUP, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

| EXAMINER |
|---|
| TSAI, H JEY |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2895 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 12/14/2009 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/710,272 | DORIS ET AL. | |
| | Examiner | Art Unit | |
| | H.Jey Tsai | 2895 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 October 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4,6,10-15 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6, 10-15, 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6, 10-15, 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Currie et al. 2004/0173812, in view of Sugii et al. 2004/0108559, or Chen et al. 2005/0242395, previously cited.

The reference discloses:

Currie et al. teaches a method of forming an electronic device, said device comprising a FinFET (Fin Field Effect Transistor) containing a plurality of fins interconnected by fin connectors (see para. 87), said method comprising:

forming at least one localized stressor region (recess) 144, 148 within said device (see figs. 10D-10E, para. 16, 77), said at least one localized stressor region 150 being located on one of said fin connectors 144, 148 (at the end of fin 18) as a region of stressor material 150 filling in an interior portion of said fin connector 144, 148 (at the end of fin 18, para. 77, 87 teach that embodiments of this invention may also be applicable to transistors with multiple or wrap-around gates. Examples of these include fin-FETs, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically), hence, the localized stressor trench region

150 (SiGe, see figure 10E) located on the fin connector (at the end of fin 18) between transistor 106 and transistor 106' can be applicable to the FinFET (Fin Field Effect Transistor). A plurality of fins 18 interconnected by fin connectors, such as fin-FETs, tri-gate FETs etc., Currie teaches: fin includes channel 108 and fin 18, fin connector/pad (source/drain) 150, gate 110, gate dielectric 114. see Chen et al. teaches in figs. 3-5, fin-FET having fin connectors 36 or S or D connecting fin 12 or 21, Sugii et al. teaches in figure 28, fin-FET having fin connectors 4 connecting fin 5.

Regarding claim 2. The method of claim 1, wherein said at least one localized stressor region 144/150 comprises a first localized stressor region 144/150, said method further comprising:

forming a second localized stressor region 148/150 within said device, said first localized stressor region and said second localized stressor region causing a region (channel) 108 there between to be stressed, para. 77, fig. 10E.

Regarding claim 3. The method of claim 2, wherein said first localized stressor region and said second localized stressor region comprise a same type material, para. 77.

Regarding claim 4. The method of claim 3, wherein said same type material comprises one of a compressive stressor material and a tensile stressor material, para. 77.

Regarding claim 6. The method of claim 2, wherein said first and second localized stressor regions are formed on said fin connectors of said FinFET as regions

of stressor material filling in interior portions of respective two fin connectors, para. 77, 87.

Regarding claim 10. The method of claim 4, wherein said same type material comprises a compressive material and primary charge carriers in said region being stressed comprise holes, para. 77, 68.

Regarding claim 11. The method of claim 4, wherein said same type material comprises a tensile material and primary charge carriers in said region being stressed comprise electrons, para. 77, 68.

Regarding claim 12. The method of claim 2, wherein said region being stressed causes a carrier mobility in said stressed region to be one of increased and decreased, relative to a carrier mobility in a region without said stress, para. 6, 35.

Regarding claim 13. The method of claim 1, wherein said device comprises one of a plurality of devices in an electronic circuit, said method further comprising: selectively providing a blocking mask 32 over devices in said electronic circuit which are not to receive said at least one localized stressor region, fig. 2.

Regarding claim 14. A method of forming a stress region in an electronic device, said device comprising a FinFET (Fin Field Effect Transistor) containing a plurality of fins interconnected by fin connectors (see para. 87 and see figs. 3-5 of Chen), said method comprising:

forming a first localized stressor region 144/150 (at the end of fin 18, see figs. 10D-10E, para. 77, 87) within said device on a first fin connector (at the end of fin 18) as comprising a first region of stressor material filling 150 in an interior portion of said first

fin connector (at the end of fin 18); and forming a second localized stressor region 148/150 within said device on a second fin connector (at the end of fin 18) as comprising a second region of stressor material 150 filling in an interior portion of said second fin connector, said first localized stressor region and said second localized stressor region causing a region 108 there between to be stressed, para. 77, 87 teach that embodiments of this invention may also be applicable to transistors with multiple or wrap-around gates. Examples of these include fin-FETs, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically), hence, the localized stressor trench region 144/150, 148/150 (see figures 10D-10E) located on the fin connector (at the end of fin 18) between transistor 106 and transistor 106' that can be applicable to the FinFET (Fin Field Effect Transistor). A plurality of fins 18 interconnected by fin connectors, such as fin-FETs, tri-gate FETs etc. Currie teaches: fin includes channel 108 and fin 18, fin connector/pad (source/drain) 150, gate 110, gate dielectric 114. see Chen et al. teaches in figs. 3-5, fin-FET having fin connectors 36 or S or D connecting fin 12 or 21, Sugii et al. teaches in figure 28, fin-FET having fin connectors 4 connecting fin 5.

Regarding claim 15. The method of claim 14, wherein said region being stressed causes a carrier mobility in said stressed region to be one of increased and decreased, relative to a carrier mobility in a region without said stress, para. 6, 35, 68.

Regarding claim 23. The method of claim 1, wherein at least one of said at least one localized stressor region 150 interacts with a stressed region 55a or 55b located outside said device, fig. 10E.

Regarding claim 24. The method of claim 1, wherein said at least one localized stressor region is used to generate one of a compression stress and a tensile stress, para. 77.

Regarding claim 25. The method of claim 1, wherein said at least one localized stressor region 150 is located within said device to generate a stress that enhances a performance of said device, para. 16, 77.

Regarding claim 26. The method of claim 25, wherein said performance enhancement comprises an increase in a carrier mobility, para. 6, 35, 77.

Regarding claim 27. The method of claim 25, wherein said performance enhancement comprises a decrease in a carrier mobility, para. 6, 35, 77.

Regarding claim 28. The method of claim 1, wherein said at least one localized stressor region is located to generate a stressed region in at least one of a direction parallel to a current flow and perpendicular to a current flow, para. 77, figs. 10E.

Regarding claim 29. The method of claim 1, wherein said at least one localized stressor region 150 is used to create a symmetrically stressed region, fig. 10E, para. 77.

Regarding claim 30. The method of claim 1, wherein said at least one localized stressor region is used to create an asymmetrically stressed region, para.77.

The difference between the reference(s) and the claims are as follows: Currie et al. teaches forming localized stressor trench regions on the fin connectors between transistors but does not show fin-FET having fin connectors in the drawing. However, Sugii et al. teaches in figure 28, fin-FET having fin connectors. Sugii et al. also teaches at figs. 13-14, 19-29, para. 123-153, the source/drain regions 4 is a part of fin connector

and forming localized stressor 5 on the of the fin connector 4. Sugii et al. also teaches forming a localized stressor 5 on the channel region, See figs. 13-14, 19-29. Chen et al. teaches at figs. 3-5 and para 26, a fin-FET having fin connectors and forming silicide layer on the fin connector.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have recognized that localized stressor trench (recess) region can be formed on a fin connector as shown in fig. 28 of Sugii et al. or figs. 3-5 of Chen et al. because fin connector connects source/drain regions of two FET transistors together.

***Conclusions***

Applicant's arguments filed Oct. 13, 2009 have been fully considered but they are not persuasive.

Applicant contends that there is no demonstration of providing a localized stressor on the fin connection of the a finFET as a filled-in region on the interior portion of the FinFET fin connectors. This is not found persuasive because Currie et al. teaches forming at least one localized stressor region (trench) 150 within said device (see fig. 10E), the at least one localized stressor region 150 being located on one of fin connectors (at the end of fin 18) connecting fin 18 as a region of stressor material filling in an interior portion of said fin connector (at the end of fin 18), para. 77. And para. 87 of Currie teach that embodiments of this invention may also be applicable to transistors

with multiple or wrap-around gates. Examples of these include fin-FETs, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically), hence, the localized stressor trench region 150 (see fig. 10E) located on the fin connector (at the end of fin 18) that is between transistor 106 and transistor 106' that can be applicable to the FinFET (Fin Field Effect Transistor). A plurality of fins 18 interconnected by fin connectors, such as fin-FETs, tri-gate FETs etc. Currie et al. teaches, the fin includes channel 108 and fin 18, fin connector/pad (source/drain) 150, gate 110, gate dielectric 114. And Chen et al. teaches in figs. 3-5, fin-FET having fin connectors 36 or S or D connecting fin 12 or 21, Sugii et al. teaches in figure 28, fin-FET having fin connectors 4 connecting fin 5.

Applicant contends that structure 18 in fig. 10D of Currie et al. is merely the lower layer of the sidewall spacer structure 120, 122. This is not found persuasive because structure 18 is a silicon fin as shown in fig. 10B-10E. Sidewall spacer structures 120, 122 are formed on sidewall of the gate electrode after forming gate electrode 110 (see para. 65). Gate electrode 110 is formed on silicon structure 18. (see para. 65).

Since, Currie et al. teaches forming localized stressor regions (see fig. 10E, 11) within the device on the fin connector as comprising of stressor material filling in an interior portion of the fin connector can be applicable to transistors with multiple or wrap-around gates. Examples of these include fin-FETs, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically), and Sugii et al. or Chen teaches a fin-FET having fin connectors, hence the combination of Currie and Sugii or Chen is proper. Therefore, it is clearly that the combination of Currie

and Sugii or Chen meets the doctrine of U.S. Supreme Court in KSR international v. Teleflex of "a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability". And, it is also clearly that the combination of Currie and Sugii or Chen meets the doctrine of U.S. Supreme Court in KSR international v. Teleflex of "If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under §103".

It is common sense that familiar items may have obvious uses beyond their primary purposes, and a person of ordinary skill often will be able to fit the teachings of multiple patents together like pieces of a puzzle. See KSR international v. Teleflex, US Supreme Court, 127 S.Ct. 1727 (2007).

More details of U.S. Supreme Court in KSR international v. Teleflex, US Supreme Court, 127 S.Ct. 1727 (2007): Granting patent protection to advances that would occur in the ordinary course without real innovation retards progress and may, in the case of patents combining previously known elements, deprive prior inventions of their value or utility. When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under §103.

When a work is available in one field, design incentives and other market forces can prompt variations of it, either in the same field or in another. If a person of ordinary skill in the art can implement a predictable variation, and would see the benefit of doing so, §103 likely bars its patentability. Moreover, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill.

It is common sense that familiar items may have obvious uses beyond their primary purposes, and a person of ordinary skill often will be able to fit the teachings of multiple patents together like pieces of a puzzle. See KSR international v. Teleflex, US Supreme Court, 127 S.Ct. 1727 (2007).

In *Sakraida* v. *AG Pro, Inc.*, 425 U. S. 273(1976), the Court derived from the precedents the conclusion that when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious. *Id.*, at 282. The principles underlying these cases are instructive when the question is whether a patent claiming the combination of elements of prior art is obvious. When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary

skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571) 272-1736.

The fax phone number for this Group is 571-273-8300.

/H.Jey Tsai/
Primary Examiner, Art Unit 2895